Improvements on a GaAs MESFET Model for Nonlinear RF Simulations

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Abstract

A modified GaAs MESFET-model has been developed to improve accuracy over a large bias range, particularly within the linear region. The enhancements consist of a modified Statz equation for the gate charge to improve the modeling of the gate drain capacitance, and an equation for the bias dependent drain source resistance for exact modeling of the dispersive output conductance.

Introduction

For the design of GaAs integrated circuits, a simple and precise simulation model is required. Analytical models [1-8] have been reported and are frequently used in common simulators. Most of these topologies use a constant, bias independent drain source resistance [1,2] to model the dispersion of the output conductance. Another approach uses an additional feedback network to distinguish between DC and AC behaviour [3,4], thereby rapidly increasing computation time and causing convergence problems. Additionally, measurements indicate that the output conductance is strongly dependent on the drain source voltage. In this approach simple equations for a bias dependent drain source resistance are proposed to model the output conductance over a large bias range with high accuracy. Furthermore the Statz gate charge formula, used in [2,3,4], is improved to better predict the gate drain capacitance C_{gd}, while the originally accurately described gate source capacitance C_{gs} remains almost unchanged. These refinements have been added to a TOM-2 model [4]. The simulations with these changes show much better agreement with measurements especially in the linear region. Thus, the new model is ideally suited for simulations of switches and mixers.

Gate Charge

The Statz equation for the gate charge is widely used in large signal models [2,3,4]. The simplicity and the strict convergence criteria for charges and capacitances make it attractive for simulators. Comparisons to measurements of ion implanted GaAs-FETs show that the bias dependence of C_{gs} is modelled correctly. But simulated values of C_{gd} deviate significantly from the measurements. In particular the Statz equations do not include the bias dependence of C_{gd} on V_{ds} > knee voltage. We propose a modified gate charge equation that improves the characteristic of C_{gd} considerably, while leaving C_{gs} almost unchanged. The modified charge equation is:

$$Q' = 2 \cdot C_{gs0} \cdot V_B \cdot \left[1 + \sqrt{1 - \frac{V_{new}}{V_B}} \right] + C_{gd0} \cdot V_B \cdot \operatorname{arsinh}\left[\frac{V_{eff_2}}{V_B} \right] \quad (1)$$

The second term of Eq. (1) is mainly responsible for C_{gd} and differs from the original Statz equation. The contribution of this term to C_{gs} is almost negligible. The derivatives of Q' with respect to the voltages V_{gs} and V_{gd} result in the capacitances C_{gs} and C_{gd}, respectively:

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$$C'_{gd} = \frac{C_{gso}}{4\cdot\sqrt{1-\frac{V_{new}}{V_B}}}\left\{1+\frac{V_{eff_1}-V_T}{\sqrt{\left(V_{eff_1}-V_T\right)^2+\delta^2}}\right\}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}+\frac{C_{gd0}}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}\frac{V_B}{\sqrt{V_{eff2}^2+V_B^2}}$$

$$C'_{gs} = \frac{C_{gso}}{4\cdot\sqrt{1-\frac{V_{new}}{V_B}}}\left\{1+\frac{V_{eff_1}-V_T}{\sqrt{\left(V_{eff_1}-V_T\right)^2+\delta^2}}\right\}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}+\frac{C_{gd0}}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}\frac{V_B}{\sqrt{V_{eff2}^2+V_B^2}}$$

(2, 3)

V_{gs}: gate source voltage
C_{gs0}: gate source capacitance for V_{gs}=0V
V_B: built in junction potential
α: drain current saturation parameter

$$V_{eff\,1} = \frac{1}{2}\left(V_{gs}+V_{gd}+\sqrt{\left(V_{gs}-V_{gd}\right)^2+\delta^2}\right)$$

$$V_{new} = \frac{1}{2}\left(V_{eff\,1}+V_T+\sqrt{\left(V_{eff\,1}-V_T\right)^2+\delta^2}\right)$$

Equations (1,2,3) fulfil the demand of charge conservation and maintain the symmetry to V_{ds}. For these monotone equations no additional parameters are needed in comparison to the Statz equations. An error function similar to the least square error was defined in Eq. (4) to compare the deviations between the simulation using either the initial Statz capacitance equations or the improved capacitance formulas and the measurements :

$$\varepsilon_{C_j} = \frac{1}{N}\sum_i\left\{\frac{\left|C_{j,meas}-C_{j,sim}\right|^2}{C_{j,meas}{}^2}\right\} \qquad (4)$$

Error values over bias range		
	ε_{Cgs}	ε_{Cgd}
Statz	0.004	0.15
this work	**0.004**	**0.003**

Tab.1

N is the number of bias points (here N=24). The values of the error function (Tab. 1) indicate that C_{gd} can be modelled more accurately with the new equations, while the accuracy of C_{gs} remains almost the same. In Fig. 4 the improved characteristic of C_{gd} is compared to both the C_{gd} obtained from the original Statz equation and from measurements.

V_{gd}: gate drain voltage
C_{gd0}: nominal gate drain capacitance
V_T: threshold voltage
δ: parameter

$$V_{eff\,2} = \frac{1}{2}\left(V_{gs}+V_{gd}-\sqrt{\left(V_{gs}-V_{gd}\right)^2+\delta^2}\right)$$

$V_{eff\ 1;2;\ new}$ as in Eq. (12a, 12b; 15) of [2]

Dispersive Drain Source Conductance

In the saturation region the DC output conductance is much smaller than the RF output conductance. A bias dependent drain source resistance R_{dis} (DC decoupled by a large capacitance C_{dis} as shown in Fig. 1) can be used to correctly model the output conductance at RF while having no effect at DC. In the linear region the DC output conductance increases and requires less compensation. Therefore R_{dis} increases. R_{dis} is modelled as follows:

$$R_{\rm dis} = R_{dis0}\cdot\left[1+\frac{1}{\left(\frac{\alpha}{2}\cdot V_{eff_3}\right)^2}\right]\cdot\left[1-\frac{V_g}{2\cdot V_{dis}}\right] \qquad (5)$$

R_{dis0}: R_{dis} for V_{gs}=0V; V_{ds}>V_{knee}
V_{dis}: compression parameter, $V_{eff\,3} = \sqrt{V_{ds}^2+\delta^2}$
V_{gs} for V_{ds} > 0V, V_{gd} for V_{ds} < 0V

Eq. (5) fulfils the demand of symmetry to V_{ds} and causes no convergence problems. The required R_{dis} for different GaAs-FETs (enhancement/depletion) can be fitted with only two extra parameters V_{dis} and R_{dis0}. As shown in Fig. 3 the extracted values from measurements agree well withEq. (5).

Model Verification

In order to verify the proposed model improvements, transistors on a standard enhancement/depletion foundry process with 0.6 µm gate length and 6 ·50 µm gate width have been measured. Large signal model parameters are extracted from small signal on wafer S-parameters and DC measurements. The equivalent large signal model used is shown in Fig. 1. Our model modifications were added to an existing TOM-2 model in a HP Libra simulator. The new model was verified through harmonics and intermodulation measurements for enhancement and depletion FETs. With the modified model the transistor behaviour can be modelled over the entire bias range (except breakdown) with high accuracy. Results are presented for an enhancement type. A typical agreement of measured and simulated small signal behaviour is shown in Fig. 2. In particular S_{12} and S_{22} are improved compared to the old model. Finally Fig. 5 and Fig. 6 compare the third order intermodulation and the harmonics at 5.2 GHz. Simulations and measurements show good agreement.

Conclusions

The linear and nonlinear high frequency performance of an existing MESFET model has been improved. A bias dependent drain source resistance is proposed to accurately model the output conductance. Furthermore the Statz equation for the gate charge description is modified to improve the characteristic of the gate drain capacitance. These refinements have been included in an existing TOM-2 model in HP Libra software. In particular the simulation accuracy for mixers and switches working in the linear region can be improved considerably. For power amplifiers the prediction of the output conductance is important for the accurate calculation of the power transferred to the load. Furthermore behaviour of oscillators can be better predicted, because it is strongly dependent on the feedback capacitanceC_{gd}.

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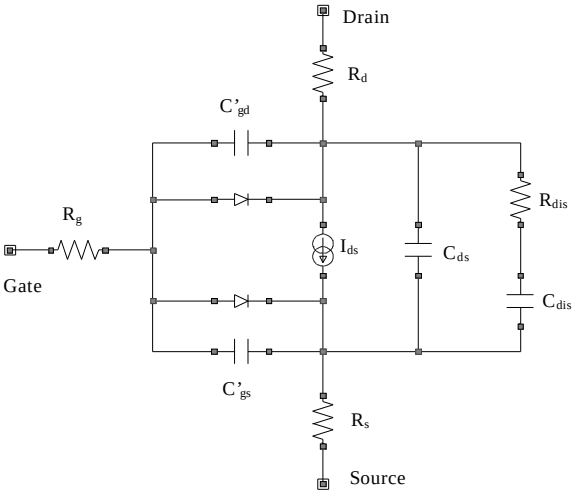

Fig. 1: Large Signal equivalent circuit

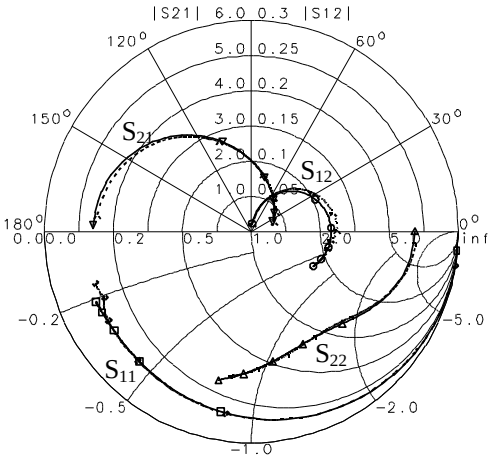

Fig. 2: S-parameters: simulated (solid) and measured (dotted), E-FET, Vds=3V, Vgs=0.4V, 0.4 GHz - 27 GHz

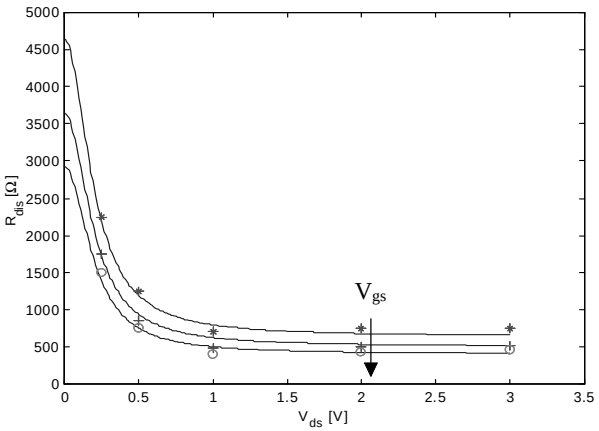

Fig. 3: Dispersion resistance R_{dis}: simulated (solid) and extracted from measurements (points), E-FET, V_{gs}=0.3, 0.4, 0.5V

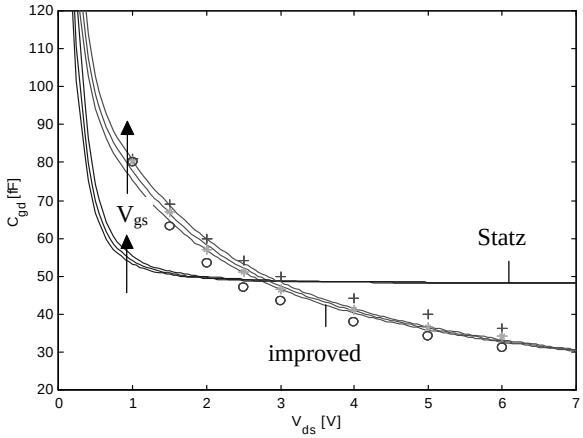

Fig. 4: Gate drain capacitance Cgd: simulations (solid) and measurements (points), E-FET, V_{gs}=0.3, 0.4, 0.5V

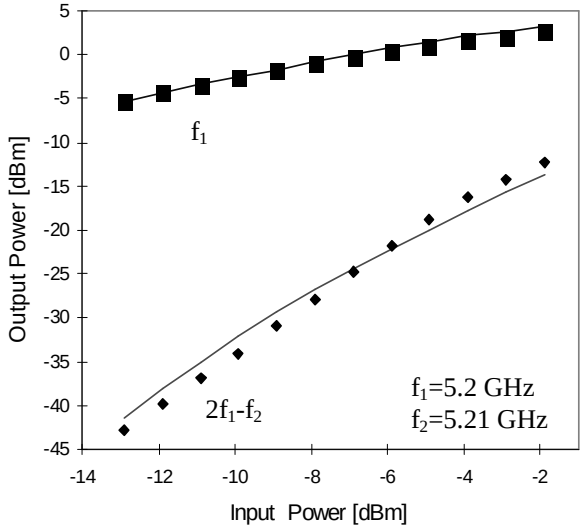

Fig. 5: Intermodulation: simulations (solid) and measurements (points), E-FET, V_{ds}=1V, V_{gs}=0.32V

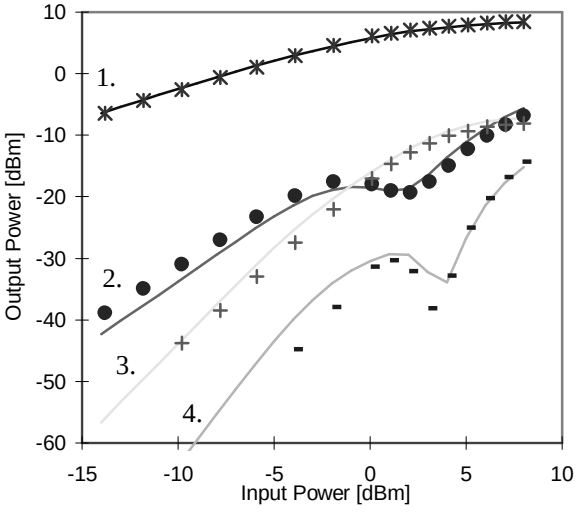

Fig. 6: Harmonics: simulations (solid) and measurements (points), E-FET, V_{ds}=1V, V_{gs}=0.32V